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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
MASKULINSKI, MICHAEL C	
ART UNIT	**PAPER NUMBER**
2113	6

DATE MAILED: 04/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/751,937	BEESLEY ET AL.	
	Examiner	Art Unit	
	Michael C Maskulinski	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 March 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *12-15* is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☒ Claim(s) *11 and 25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Final Office Action

Claim Rejections - 35 USC § 103

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

2. Claims 1-10, and 16-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Evans et al., U.S. Patent 5,163,052, and further in view of Microsoft Press Computer Dictionary.

Referring to claim 1:

a. In the Abstract, Evans et al. disclose a multiple-board computer system (a plurality of processors implemented on at least two circuit boards).

b. In column 3, lines 30-41, Evans et al. disclose two redundant diagnostic processor boards, which monitor and control the operation of the system processor board and system memory board MCUs. However, Evans et al. don't explicitly disclose each of the plurality of processors implementing diagnostic access functions before the processor is fully on-line. On page 376, the Microsoft Press Computer Dictionary discloses a power-on self test which is a set of routines stored in a computer's read-only memory that tests various system components such as RAM, the disk drives, and the keyboard to see if they are properly connected and operating (diagnostic access functions). If the power-on self test is successful, it passes control to the system's bootstrap loader (before the processor is fully on-line). It would have been obvious to one of ordinary skill at the time of the invention to include the power-on self test of Microsoft Press

Computer Dictionary into the system of Evans et al. A person of ordinary skill in the art would have been motivated to make the modification because it provides a means of fault avoidance and insures that the computer system is operating properly.

c. In column 3, lines 30-41, Evans et al. disclose a serial diagnostic bus and bus interface module. A plurality of receiver/driver circuits each connected to a serial port of one of the plurality of processors are inherent to the system of Evans et al.

d. In column 3, lines 30-41, Evans et al. disclose two redundant diagnostic processor boards, which monitor and control the operation of the system processor board and system memory board MCUs. Strictly speaking, the diagnostic processor board "listens" for problems with the diagnostic processor board and is only operational when the diagnostic processor board is malfunctioning (a master processor coupled to the receiver/driver circuits to select one of the plurality of processors as an active processor for communicating diagnostic information to the master processor by instructing the receiver/driver circuit associated with the selected processor to logically connect the selected processor to the master processor).

e. In Figure 2, Evans et al. disclose a bus connecting the master processor to the receiver/driver circuits.

Referring to claim 2, in column 1, lines 46-53, Evans et al. disclose that the computer system has at least one system processor board, the components of the

system processor board being inter alia, at least one CPU for controlling the operation of the system processor board (wherein each of the plurality of processors is a control processor for one of the circuit boards).

Referring to claims 3, 17, and 19, in the Abstract, Evans et al. disclose a multiple board computer system. However, Evans et al. don't explicitly disclose that the circuit boards are each inserted into a physical housing. The Examiner takes Official Notice that in the art of computer systems it is well known to insert circuit boards into a physical housing. An example of this is a sound card or an Ethernet card. It would have been obvious to one of ordinary skill at the time of the invention to include the insertion into a physical housing into the system of Evans et al. A person of ordinary skill in the art would have been motivated to make the modification because inserting the circuit boards into a physical housing mounts them so they can't move and it is a means of powering them.

Referring to claim 4, in Figure 2, Evans et al. disclose a bus separate from the processor boards (the bus is implemented in the physical housing).

Referring to claim 5, in the Abstract, Evans et al. disclose a multiple board computer system. However, Evans et al. do not disclose the function of the computer system. The Examiner takes Official Notice that in the art of networks it is well known to have circuit boards and computer systems perform the operations in a network router. It would have been obvious to one of ordinary skill at the time of the invention to use the computer system of Evans et al. as a network router. A person of ordinary skill in the art would have been motivated to make the modification because by definition a router

is a device that can forward packets from one device on a network to another device and a computer system is capable of performing this function.

Referring to claim 6, in column 3, lines 30-41, Evans et al. disclose a serial diagnostic bus and bus interface module. Further, in column 3, lines 42-44, Evans et al. disclose that the MCU constantly monitors the MCU's on the system processor boards and on the system memory board by receiving status information. In other words, the diagnostic MCU constantly queries the other MCU's as to whether problems exist upon the other boards (control logic connected to the master processor and the receiver/driver circuits, the control logic activating, based on commands from the master processor, the selected one of the receiver/driver circuits and deactivating non-selected ones of the receiver/driver circuits). Further, in column 5, lines 4-7, Evans et al. disclose that the diagnostic bus is used for controlling the operation of an MCU on a system board when that system board is determined by its MCU to be malfunctioning.

Referring to claims 7 and 21, in column 5, lines 4-7, Evans et al. disclose that the diagnostic bus is used for controlling the operation of an MCU on a system board when that system board is determined by its MCU to be malfunctioning. However, Evans et al. don't explicitly disclose that the non-selected MCU's present high-impedance states to the bus. The Examiner takes Official Notice that in the art of buses it is well known to present a high-impedance state to a bus in order to disconnect a device from the bus. It would have been obvious to one of ordinary skill at the time of the invention to have the non-selected MCU's present high-impedance states to the bus to disconnect them. A person of ordinary skill in the art would have been motivated to make the modification

because a high-impedance state basically creates an open circuit; therefore, the device appears disconnected.

Referring to claim 8, in Figure 2, Evans et al. disclose in reference numbers 260 and 270 an additional receiver/driver circuit connecting the master processor to the bus.

Referring to claims 9, 10, 23, and 24, in Figure 2, Evans et al. disclose the plurality of receiver/driver circuits and the additional receiver/driver circuit. However, Evens et al. don't explicitly disclose that they communicate using TTL signals, and a signal converter connected between the additional receiver/driver circuit and the master processor, the signal converter converting TTL signals for the additional receiver/driver circuit to RS-232 signals for the master processor. The Microsoft Press Computer Dictionary defines TTL as a type of bipolar circuit design that utilizes transistors connected to each other either directly or through resistors. Further, the Microsoft Press Computer Dictionary defines RS-232 as an accepted industry standard for serial communications connections. It would have been obvious to one of ordinary skill at the time of the invention to include the TTL signals, RS-232 signals, and the signal converter into the system of Evans et al. A person of ordinary skill in the art would have been motivated to make the modification because transistor-transistor logic (TTL) offers high speed and good noise immunity and is used in many digital circuits (see Microsoft Press Computer Dictionary: page 475). Further, RS-232 and TTL are well known and accepted standards and choosing to use them is a design choice.

Referring to claim 16:

a. In Figure 2, Evans et al. disclose a bus.

b. In the Abstract, Evans et al. disclose a multiple-board computer system (a packet forwarding engine having a plurality of circuit boards each including at least one processor). In column 3, lines 30-41, Evans et al. disclose a serial diagnostic bus and bus interface module. A receiver/driver circuit associated with each of the processors is inherent to the system of Evans et al.

c. In column 3, lines 30-41, Evans et al. disclose two redundant diagnostic processor boards, which monitor and control the operation of the system processor board and system memory board MCUs. However, Evans et al. don't explicitly disclose that each of the processors is configured to implement low-level diagnostic access functions before the packet forwarding engine is fully on-line. On page 376, the Microsoft Press Computer Dictionary discloses a power-on self test which is a set of routines stored in a computer's read-only memory that tests various system components such as RAM, the disk drives, and the keyboard to see if they are properly connected and operating (diagnostic access functions). If the power-on self test is successful, it passes control to the system's bootstrap loader (before the packet forwarding engine is fully on-line). It would have been obvious to one of ordinary skill at the time of the invention to include the power-on self test of Microsoft Press Computer Dictionary into the system of Evans et al. A person of ordinary skill in the art would have been motivated to make the modification because it provides a means of fault avoidance and insures that the computer system is operating properly.

d. In column 3, lines 30-41, Evans et al. disclose two redundant diagnostic processor boards, which monitor and control the operation of the system processor board and system memory board MCUs. Strictly speaking, the diagnostic processor board "listens" for problems with the diagnostic processor board and is only operational when the diagnostic processor board is malfunctioning (a routing engine, connected to the bus, including a master processor selecting one of the of processors as an active processor for communicating diagnostic information by instructing the receiver/driver circuit associated with the selected processor to logically connect the selected processor to the bus).

e. In the Abstract, Evans et al. disclose a multiple board computer system. However, Evans et al. do not disclose the function of the computer system. The Examiner takes Official Notice that in the art of networks it is well known to have circuit boards and computer systems perform the operations in a network router. It would have been obvious to one of ordinary skill at the time of the invention to use the computer system of Evans et al. as a network router. A person of ordinary skill in the art would have been motivated to make the modification because by definition a router is a device that can forward packets from one device on a network to another device and a computer system is capable of performing this function.

Referring to claim 18, in column 1, lines 46-53, Evans et al. disclose that the computer system has at least one system processor board, the components of the

system processor board being inter alia, at least one CPU for controlling the operation of the system processor board (wherein each of the plurality of processors is a control processor for one of the circuit boards).

Referring to claim 20, in column 3, lines 30-41, Evans et al. disclose a serial diagnostic bus and bus interface module. Further, in column 3, lines 42-44, Evans et al. disclose that the MCU constantly monitors the MCU's on the system processor boards and on the system memory board by receiving status information. In other words, the diagnostic MCU constantly queries the other MCU's as to whether problems exist upon the other boards (control logic connected to the master processor and the receiver/driver circuits, the control logic activating, based on commands from the master processor, the selected one of the receiver/driver circuits and deactivating non-selected ones of the receiver/driver circuits). Further, in column 5, lines 4-7, Evans et al. disclose that the diagnostic bus is used for controlling the operation of an MCU on a system board when that system board is determined by its MCU to be malfunctioning.

Referring to claim 22, in Figure 2, Evans et al. disclose in reference numbers 260 and 270 an additional receiver/driver circuit connecting the master processor to the bus.

Allowable Subject Matter

3. Claims 11 and 25 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including **all** of the limitations of the base claim and any intervening claims.

4. Claims 12-15 are allowed.

5. The following is a statement of reasons for the indication of allowable subject matter: referring to claims 11, 12, and 25, the prior art does not teach or reasonably suggest the boot code permitting each of the plurality of processors to transmit diagnostic information before the boot code is fully loaded.

Response to Arguments

6. Applicant's arguments, see paper no. 5, filed March 11,2004, with respect to the rejection(s)of claim(s) 1, 2, 6, 8 under 35 U.S.C. 102(b) as being anticipated by Evans et al., U.S. Patent 5,163,052 and the rejection of claims 3, 4, 5, 7, and 16-22 under 35 U.S.C. 103(a) as being unpatentable over Evans et al., U.S. Patent 5,163,052 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Microsoft Press Computer Dictionary.

7. The Examiner would like to remind the applicant that claims 1 and 16 would be allowable if they were re-written to include all of the limitations of claims 11 and 25.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael C Maskulinski whose telephone number is (703) 308-6674. The examiner can normally be reached on Monday-Friday 9:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W Beausoliel can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MM

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